REMARKS

Reconsideration of the subject application as amended herein is respectfully requested.

In the outstanding Office Action, the Examiner rejected independent Claims 1 and 4 under 35 U.S.C. §103(e) as being anticipated by Kumar et al. The Examiner found the remaining claims allowable. The Applicants respectfully traverse the rejections.

1. The claimed invention

As set forth in independent claims 1 and 4, in the present invention the packets of a sequence are stowed away in a packets memory organized as a stack, in association with respective processing labels. The processing label associated with each packet extracted from the packets memory is examined so as to activate a processing module selected as a function of the label received. The activated module performs an elementary processing of the packet extracted.

The elementary processing performed by at least one of the processing modules comprises associating the extracted packet with a label modified in accordance with a labels translation table, the processed packet subsequently being stowed away again in the packets memory in association with the modified label.

2. The claimed invention is patentably distinguishable over Kamar et al:

Kamar et al. discloses, as shown in figure 1, an interface (ALI), to be connected to the input (ALI 14, 15, 16) or the output (ALI 23, 24, 25) of a cell switch 10. Such an interface is adapted to realize in an unified way, some tasks that, in the prior art, were operated by several devices. These tasks deal with, for example, changing cell header, appending a local cell header, policing traffic flow, extracting/inserting cells in the flow, etc.

The Examiner states that col. 4 lines 51-65 and col. 7 lines 47-67 anticipate the last feature of the invention (" the elementary processing ... modified label"). In col. 4 lines 51-65, Kumar et al. discloses that in ALI located at the output of the switch, such as ALI 23, 24, 25, several processes are realized, that modify some fields in the cell headers relative to the HEC, ATM header and local header. Col. 7 lines 47-67 details the modification of the ATM header: some bits of the current header are changed with corresponding bits of a new header, the bits to be changed being indicated by a mask register.

Thus, the Examiner seems to compare some processing modules of the invention to the processes of changing field in the headers of the cell and to equate the current header of Kumar with the current label and the modified header with the modified label. Further he seems to equate the mask register to the label translation table.

However, the modified cell header (or the current cell header), is not a label such that a processing module among a plurality of processing modules can be selected as a function of the label, as recited in the independent Claims 1 and 4. Indeed, cell headers are not processing labels, aimed to indicate a

particular module among several modules, to be processed about the cell, but they are content labels, modified according to predefined configuration (mask register). Therefore, the independent Claims 1 and 4 of the invention, that enable a great flexibility of the configuration of the process applied to the sequence of packets, is not disclosed by Kumar et al.

Consequently, it is requested that the 35 U.S.C §102 rejection of Claims 1 and 4 be reconsidered, and that these claims be allowed.

New claim 6 contains the limitations of claims 1 and 2, new claim 7 is identical to claim 3 except that it depends on claim 6 and new claim 8 contains the limitations of claims 4 and 5. Since the Examiner has indicated that claims 2, 3 and 5 contain allowable subject matter, it is respectfully submitted that these claims are allowable.

In light of the foregoing, the prompt issuance of a notice of allowance is respectfully requested.

Respectfully submitted

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